UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte KEITH DOW

Appeal No. 2005-0892
Application No. 09/461,643

ON BRIEF

Before GROSS, LEVY, and BLANKENSHIP, Administrative Patent Judges.
LEVY, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134 from the examiner's final rejection of claims 1, 3-8, 10-14, 16-20, 23 and 24, which are all of the claims pending in this application.

BACKGROUND

Appellant's invention relates to signal routing between a memory control unit and a memory device. An understanding of the invention can be derived from a reading of exemplary claim 20, which is reproduced as follows:

> 20. A circuit board comprising at least two layers formed in parallel to a surface of said circuit board for use in a computer system comprising:
>
> a memory unit;
>
> a memory control unit; and
>
> a data bus connecting the memory control unit to the memory unit and comprising:
>
> a first signal line formed on a first layer of the circuit board and connected to the memory control unit and to a first pin on the memory unit, and
>
> a second signal line formed on the first layer of the circuit board and also connected to the first pin connection on the memory unit , a first portion of the second signal line at an acute angle relative to a first portion of the first signal line, a second portion of the second signal line substantially parallel to a second portion of the first signal line,
>
> wherein the widths of the lines and a perpendicular distance separating the second portions of the lines are each substantially equal, and
>
> wherein said first layer defines a non-grounded gap between said first and second portions of the first and second lines.

The prior art references of record relied upon by the examiner in rejecting the appealed claims are:

Theus	4,904,968	Feb. 27, 1990
Perino et al. (Perino)	6,160,716	Dec. 12, 2000 (filed Jun. 25, 1999)

Appellant's Admitted Prior Art (AAPA)

Claims 1, 4-8, 11-14, 16-20, 23 and 24 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Appellant's Admitted Prior Art (AAPA) in view of Perino.

Claims 3 and 10 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over AAPA in view of Perino and Theus.

Rather than reiterate the conflicting viewpoints advanced by the examiner and appellant regarding the above-noted rejections, we make reference to the examiner's answer (mailed April 30, 2004) for the examiner's complete reasoning in support of the rejections, and to appellant's brief (filed March 15, 2004) and reply brief (filed July 6, 2004) for appellant's arguments thereagainst. Only those arguments actually made by appellant have been considered in this decision. Arguments which appellant could have made but chose not to make in the brief have not been considered. See 37 CFR § 41.37(c)(1)(vii).

OPINION

In reaching our decision in this appeal, we have carefully considered the subject matter on appeal, the rejections advanced by the examiner, and the evidence of obviousness relied upon by the examiner as support for the rejections. We have, likewise, reviewed and taken into consideration, in reaching our decision, appellant's arguments set forth in the briefs along with the examiner's rationale in support of the rejections and arguments in rebuttal set forth in the examiner's answer.

Upon consideration of the record before us, we reverse, for the reasons set forth by appellant. We begin with claim 20 (brief, page 4).

In rejecting claims under 35 U.S.C. § 103, it is incumbent upon the examiner to establish a factual basis to support the legal conclusion of obviousness. See In re Fine, 837 F.2d 1071, 1073, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). In so doing, the examiner is expected to make the factual determinations set forth in Graham v. John Deere Co., 383 U.S. 1, 17, 148 USPQ 459, 467 (1966), and to provide a reason why one having ordinary skill in the pertinent art would have been led to modify the prior art or to combine prior art references to arrive at the claimed invention. Such reason must stem from some teaching, suggestion

or implication in the prior art as a whole or knowledge generally available to one having ordinary skill in the art. Uniroyal, Inc. v. Rudkin-Wiley Corp., 837 F.2d 1044, 1051, 5 USPQ2d 1434, 1438 (Fed. Cir. 1988); Ashland Oil, Inc. v. Delta Resins & Refractories, Inc., 776 F.2d 281, 293, 227 USPQ 657, 664 (Fed. Cir. 1985); ACS Hosp. Sys., Inc. v. Montefiore Hosp., 732 F.2d 1572, 1577, 221 USPQ 929, 933 (Fed. Cir. 1984). These showings by the examiner are an essential part of complying with the burden of presenting a prima facie case of obviousness. Note In re Oetiker, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992). If that burden is met, the burden then shifts to the applicant to overcome the prima facie case with argument and/or evidence. Obviousness is then determined on the basis of the evidence as a whole. See id.; In re Hedges, 783 F.2d 1038, 1039, 228 USPQ 685, 686 (Fed. Cir. 1986); In re Piasecki, 745 F.2d 1468, 1472, 223 USPQ 785, 788 (Fed. Cir. 1984); and In re Rinehart, 531 F.2d 1048, 1052, 189 USPQ 143, 147 (CCPA 1976).

The examiner takes the position (answer, page 3) that in AAPA, both the first and second signal lines are on the same first layer of the circuit board. Appellant asserts (reply brief, page 1) that there is no such teaching found in the AAPA. It is argued (id.) that in AAPA, the signal lines often must be

formed on different layers of the circuit board. From our review of the specification, we find (page 2) that:

> Fig. 2 shows a common routing configuration for signal lines connecting the MCU 120 to the memory unit. Each signal line 150 leaves the MCU 120 with a width of approximately 18 mils. Before reaching the appropriate pin 155 on the memory unit, the signal line 150 narrows, or "necks down", to a width of approximately 5 mils. The signal line 160 exiting the pin 155 also has a width of approximately 5 mils before expanding to a width of approximately 18 mils. A ground trace 165 separates the 5 mil neck down portions of the signal lines 150, 160. As a result of this congestion, the signal line 150 into the memory unit and the signal line 160 out of the memory unit often must be formed on different layers of the circuit board on which the MCU and memory unit reside.

From the disclosure that the signal lines "must often be formed on different layers of the circuit board," we find that "often" does not mean "always," and conclude that from the specification, in at least some instances, the signal lines will be formed on the same layer of the circuit board. Thus, we find that the AAPA teaches or suggests having both signal lines on the same layer of the circuit board.

From our review of Perino, we find, for the reasons which follow, no teaching or suggestion of modifying AAPA to provide "a second portion of the second signal line substantially parallel

to a second portion of the first signal line," as recited in independent claim 20. Perino is directed to providing a motherboard with "one-between" trace connections. Although example B in figure 8 appears to disclose traces 870 and 880 to be substantially parallel to each other, from Perino's lack of any disclosure of having plural traces connect to the same pin, we find no reason to replace the acute angled second portions of the traces of figure 2 of AAPA with substantially parallel portions as claimed. In addition, Perino discloses (col. 2, lines 15-29) that:

> Closely spaced traces, 130 may cause interference in some instances, or actual contact between the traces 130 if the traces are imperfectly fabricated. The trace pattern illustrated in FIG. 4 is one prior art trace pattern. As can be seen, the trace pattern has two signal traces 130 crossing between two contact areas 440 at location 490. This is called "two-between routing." Using "two-between routing" may cause interference between the signals carried by either of the traces. Furthermore, having two traces between the contact areas requires the use of thinner traces, to fit the traces between the contact area spacing. Additionally, thin traces have an increased impedance, that does not match the impedance of the signals from the daughter board. Impedance mismatch causes reflected signals, thus degrading signal integrity and limiting operating frequency.

Because the closely spaced traces of figure 2 of the AAPA may require the traces to be on different layers due to congestion

(specification, page 2), we find that the congestion may cause interference in the AAPA. As closely spaced traces create "two-between" routing, we find no suggestion to provide the AAPA with the two-between routing shown in figure 8, example B of Perino.

In addition, Perino discloses (col. 5, lines 19-32) that in figure 8, example A illustrates minimizing the distances between traces 830 and 840 and contact areas 810 and 820, while maximizing the width of the width of traces 830 and 840. Perino further discloses that maximizing the width of the traces decreases the impedance of the traces 830 and 840. Reducing the impedance of the traces to match low impedance lines/signals is advantageous because a matched impedance eliminates reflected signals, and signal deterioration. If, for the sake of argument, an artisan were taught to modify the trace lines of the AAPA to have second portions that were substantially parallel, as in figure 8, example A of Perino, an artisan wold have been taught to make the traces wider. However, in AAPA the second portions of the traces cannot be made wider because of the congestion. Thus, we find that an artisan would not have been taught to modify the AAPA to result in the claimed invention. We add that in figure 8, example B a different spacing example shown

where the widths of the spacings were decreased from 12.5 mil (example 8A) to 8 mil. However, this results in an increased impedance (45 ohms in example A to 55 ohms in example B). Because reduced impedance (not increased impedance) is advantageous, we find that an artisan would not have modified the AAPA with figure 8, example B of Perino, as advanced by the examiner.

Moreover, Perino discloses that in some instances, signal trace areas can interfere with each other, and that such signal interference is known in the art. It is disclosed that one method of preventing interference is to provide ground traces between the signal traces (see figure 11). "Thus, by placing ground traces 1160, coupling ground contact areas 1130 to 1155 and 1135 to 1150, between the signal traces 1170, noise is reduced" (col. 6, lines 10-21). From this disclosure, we find a teaching to provide ground traces between the signal traces in order to prevent interferences. Thus, since the AAPA discloses a ground trace 165 between the signal traces and 160, we find that an artisan would not have been motivated to delete the ground trace of AAPA and define a non-grounded gap between the

first and second portions of the first and second signal lines. In addition, as to the examiner's reliance on figure 16 of Perino (answer, page 4) we find that Perino does disclose a one-between connection where the opposite side of the motherboard can have the ground connection (col. 7, lines 48-50). However, we find no teaching of having substantially parallel second portions of the first and second signal lines. Nor do we find, for the reasons, supra, of any motivation for modifying AAPA to provide AAPA with substantially parallel second portions on the first and second signal lines.

Although we agree with the examiner (answer, page 4) that since Perino suggests the use of a ground contact between signal lines if the signal lines may cause interferences, if there were no interferences between the signal lines a ground may not be needed. However, due to the congestion of the signal lines of the AAPA, we find that interference could occur and that the ground, disclosed by AAPA was needed. Thus, an artisan would have been motivated to provide a non-grounded gap between the signal lines.

We are not persuaded by the examiner's assertion (answer, page 16) that example B of figure 8 of Perino achieves the

advantages of eliminating reflected signals and signal deterioration caused by mismatched impedance because example B is a showing of mismatched impedance in a prior art spacing example.

Moreover, although we agree with the examiner's assertion (answer, page 17) to the effect that in Perino, a ground trace is not needed if there is a large spacing between the signal lines (and there is no need for signal isolation), because we find that in AAPA, congestion exists where the signal lines meet the pin connector 155 of memory (or repeater hub) 110, we find that a ground trace is needed.

From all of the above, we agree with appellant that the teachings of AAPA and Perino would not have suggested to an artisan the invention set forth in claim 20. In addition, as independent claims 1, 8 and 14 also recite, at least, that the second portions of the signal lines are substantially parallel, we find that the examiner has failed to establish a prima facie case of obviousness of independent claims 1, 8 and 14. Accordingly, the rejection of claims 1, 4-8, 11-14, 16-20, 23 and 24 under 35 U.S.C. § 103(a) is reversed.

We turn next to the rejection of claims 3 and 10 under 35 U.S.C. § 103(a) as being unpatentable over AAPA in view of Perino and Theus. We cannot sustain the rejection of claims 3 and 10

because the examiner has failed to show how Theus makes up for the deficiencies of AAPA and Perino. Accordingly, the rejection of claims 3 and 10 under 35 U.S.C. § 103(a) is reversed.

CONCLUSION

To summarize, the decision of the examiner to reject claims 1, 3-8, 10-14, 16-20, 23 and 24 under 35 U.S.C. § 103(a) is reversed.

REVERSED

ANITA PELLMAN GROSS
Administrative Patent Judge

STUART S. LEVY
Administrative Patent Judge

HOWARD B. BLANKENSHIP
Administrative Patent Judge

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